# A Spiral Approach to Teaching Jitter Analysis in the Undergraduate Curriculum

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**Abstract:** Timing jitter is the phenomenon of a digital waveform's transition appearing before or after the expected time. It has been an increasingly significant problem in the high-speed electronics industry during the last decade. As such, it seems appropriate to introduce the subject of jitter analysis to electrical engineering and electrical engineering technology students as part of the undergraduate curriculum. If the subject matter is split into blocks, it can be introduced using a "spiral" approach that introduces a few topics at a time and spreads the instruction across several courses. This technique makes it easier to incorporate the material into a curriculum and should enhance student retention.

**Acronyms:**

| | | | |
|---|---|---|---|
| BERT | bit error ratio (or rate) tester | PCB | printed circuit board |
| BJT | bipolar junction transistor | PDF | probability density function |
| BW | bandwidth | PRBS | pseudo-random binary sequence |
| CDF | cumulative distribution function | PJ | periodic jitter |
| DCD | duty cycle distortion | RJ | random jitter |
| DDR | double data rate | RF | radio frequency |
| DJ | deterministic jitter | RMS | root-mean-square |
| DSO | digital storage oscilloscope | SSCG | spread spectrum clock generation |
| EE | electrical engineering | SR | slew rate |
| EET | electrical engineering technology | TIA | time interval analyzer |
| EMI | electromagnetic interference | TIE | time interval error |
| ISI | intersymbol interference | TJ | total jitter |
| MOSFET | metal oxide silicon field effect transistor | UI | unit interval |

## I. Introduction

Timing jitter is an undesirable attribute of all digital systems (general purpose computers, microcontrollers, routers, switches, cell phones, etc.). It affects virtually all communications links, whether a long-haul fiber optic link or a trace between two chips on a PCB, and whether point-to-point or a shared bus. Learning how to reduce it has become a critical skill for many system designers. This article begins with background about jitter's basic characteristics, how it

is measured and displayed, and the tools used to analyze it. Then, it proposes a three-phase spiral approach to teaching jitter analysis in the electrical engineering (EE) or electrical engineering technology (EET) curriculum.

Timing jitter is defined as the short-term (i.e., freq ≥ 10 Hz) variations of the significant instants of a timing signal from their ideal positions in time [1]. These "significant instants" are generally the digital signal transitions, or rising/falling edges. If a given transition is displaced enough that it happens in a different clock cycle, a data error occurs on the bus. Thus, for the sake of bus accuracy, it is preferable that the magnitude of jitter be negligible compared to the clocking period. Unfortunately, this is at odds with the goal of ever-increasing data rates. If the data rate of a bus is increased (with no other changes to the system), then the magnitude of jitter in time stays approximately the same, while its proportion of the bit period increases. With the constant pressure for higher speeds in modern bus architectures, it is important to balance these two competing demands, in order to maximize speed while meeting data accuracy goals. Moreover, many new bus specifications include jitter tolerances [2, 3, 4, 5, 6, 7, 8]. Thus, understanding jitter has become very important for today's digital system designers.

Like a lot of troubleshooting, correctly analyzing jitter and fixing the causal problem(s) can be very challenging. It starts with understanding the nature of jitter itself, and what causes each type of jitter. Next, one must choose not only the right piece of test equipment to measure it, but also which measurements to make, how to display them, and then apply the right techniques to isolate the underlying problem(s).

The following four sections provide background on various aspects of jitter: its basic nature, how it is measured, how the measurements can be displayed, and some useful test instruments. The next section proposes a spiral approach to weave jitter topics into an EE or EET curriculum. The conclusion summarizes the work done so far and possible future work.

## II. Jitter Basics

Jitter has two fundamental components: random (RJ) and deterministic (DJ). RJ is usually caused by thermal effects or other events that may be largely beyond the designer's control. Because of its random nature, RJ's measurement magnitudes have a Gaussian distribution with respect to time, are theoretically unbounded, and are expressed as RMS (root-mean-square) values. Deterministic jitter is generally caused by phenomena that the designer can control, at least to some extent. If this DJ can be accurately analyzed and traced to its source, it can often be significantly reduced. DJ is also somewhat more intuitive because it is bounded, and the measurements are expressed in peak-to-peak terms. Peak-to-peak jitter (in seconds) is calculated in a very simple and direct way, as shown in Equation (1).

$$DJ_{pp} = DJ_{max} - DJ_{min} \quad (1)$$

RMS jitter, in seconds, is calculated using standard statistics for discrete measurements:

$$RJ_{rms} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(RJ_i - \mu)^2} \tag{2}$$

where μ is the expected time of the waveform transition in seconds, $RJ_i$ is actual time of the ith transition in seconds, and N is the total number of transitions measured.

Total jitter (TJ), which is what can be measured in real circuits, is a combination of random and deterministic jitter, also in seconds. More specifically, it is the convolution of the RJ and DJ:

$$TJ = RJ * DJ. \tag{3}$$

For example, Figure 1 illustrates a notional measurement of (total) jitter. Its bimodal distribution, which is obviously not Gaussian, is a clear indication of DJ. It is actually a combination of the Gaussian, or normal, distribution of RJ shown in Figure 2 and the DJ distribution shown in Figure 3. Although the TJ contains DJ, the two "humps" in the graph are normally distributed. If the RJ and DJ distributions (Figure 2 and Figure 3, respectively) are convolved, the result is the TJ distribution of Figure 1. Of prime importance, however, is the fact that there are techniques to do the reverse: separate the RJ and DJ components. Mathematical algorithms can be applied to characterize those components (e.g., for compliance testing); and live measurement techniques can isolate specific types of DJ for troubleshooting in the lab. The form of DJ depicted in this case is periodic jitter, which will be covered in the following paragraphs.

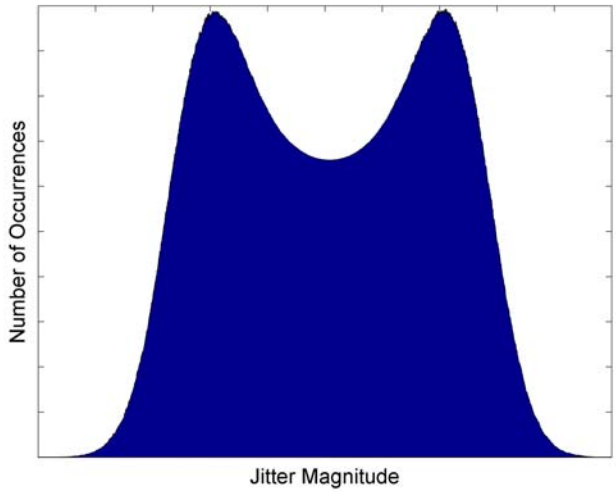


**Figure 1: Histogram of total jitter, including both random and deterministic components**

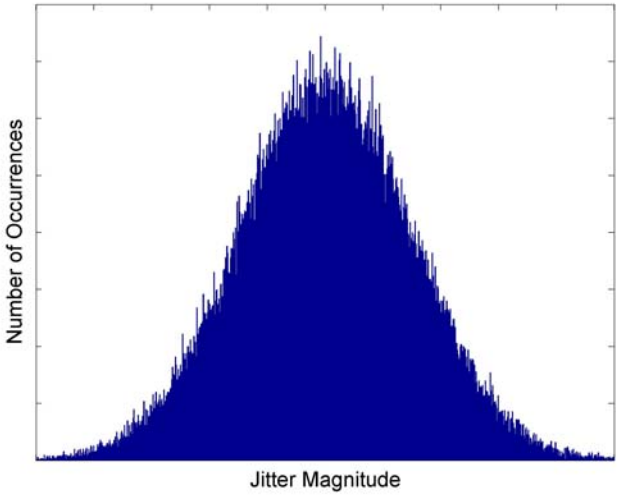


**Figure 2: Random component of total jitter measurement shown in Figure 1**

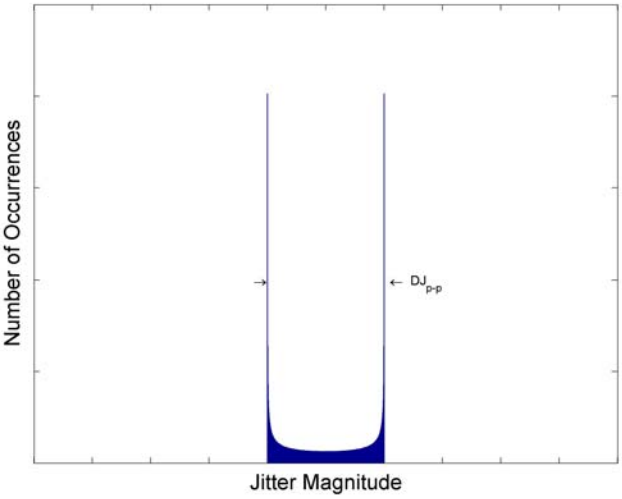


**Figure 3: Deterministic component of total jitter measurement shown in Figure 1**

There are three basic types of deterministic jitter: duty cycle distortion (DCD), intersymbol interference (ISI), and periodic jitter (PJ) [9]. DCD can be caused by two different conditions: incorrect voltage threshold and asymmetric edge rates. An incorrect voltage threshold changes the pulse width of a waveform, even if the edge rates are symmetric. If the threshold is set too high, it makes the positive pulses narrower and the negative pulses wider. From a jitter perspective, this translates into positive jitter on the rising edges and negative jitter on the falling edges. This is illustrated in Figure 4, which shows the received waveform and correct threshold level in solid black; the distorted interpretation of the received waveform, caused by its threshold being set too high, in dashed red; the correct transition times in dotted black; and the incorrectly interpreted transition times in dotted red.

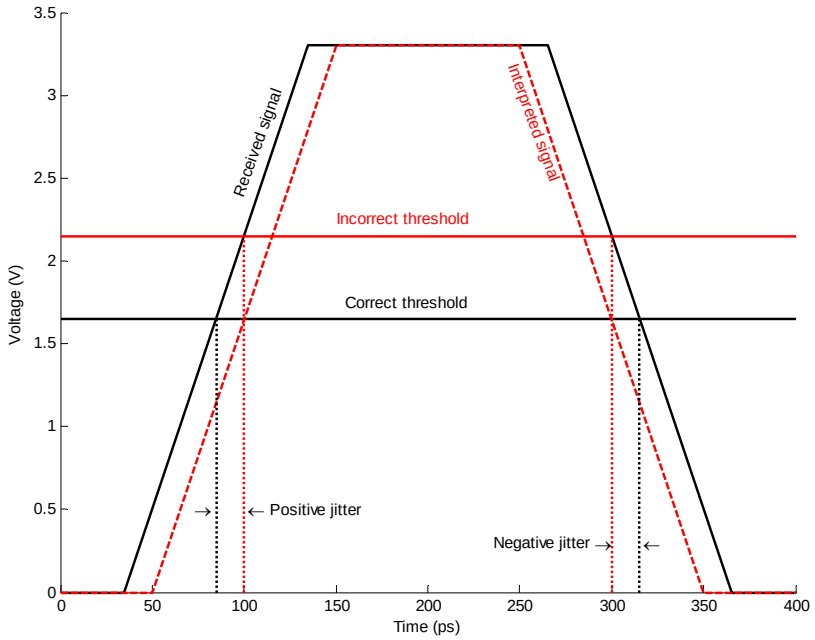


**Figure 4: Duty cycle distortion caused by incorrect receiver threshold**

The quantity of timing jitter induced by an incorrect threshold setting is roughly proportional to the rise or fall time of the signal. A good approximation of induced jitter can be made by assuming a linear signal transition, so the slew rate is given by

$$SR = \frac{\Delta v}{\Delta t} = \frac{0.8(V_H - V_L)}{t_r}, \tag{4}$$

where SR is the transition slew rate in volts per microsecond, $V_H$ is the signal's high voltage in volts, $V_L$ is the signal's low voltage in volts, and $t_r$ is the rise time (which could be replaced by $t_f$, the fall time, for a negative-going transition) in microseconds. The "0.8" multiplier comes from the conventional definition of rise (or fall) time, which is the time it takes for a signal transition to go from 10% to 90% of its peak value ($V_H$ in this case) [10]. The relationship between the magnitude of error in threshold voltage setting and induced jitter is then

$$DCD = \frac{V_{T\_error}}{SR}, \tag{5}$$

where DCD is the induced jitter magnitude in seconds and $V_{T\_error}$ is the amount of error in the threshold voltage setting in volts. Substituting Equation 4 into Equation 5 gives the induced duty cycle distortion in terms of the rise time, threshold voltage error, and high/low signal voltages:

$$DCD = t_r \frac{V_{T\_error}}{0.8(V_H - V_L)}. \tag{6}$$

On the other hand, it is possible for different edge rates on the rising and falling edges of a digital waveform to cause DCD jitter, even if the voltage threshold is set correctly [9]. For instance, if the rise time is significantly faster than the fall time, this would widen the positive pulses and narrow the negative pulses. Such a condition translates into negative jitter on the rising edges and positive jitter on the falling edges. Recovering the ideal clock signal is useful for quantifying this type of DCD, which is depicted in Figure 5.

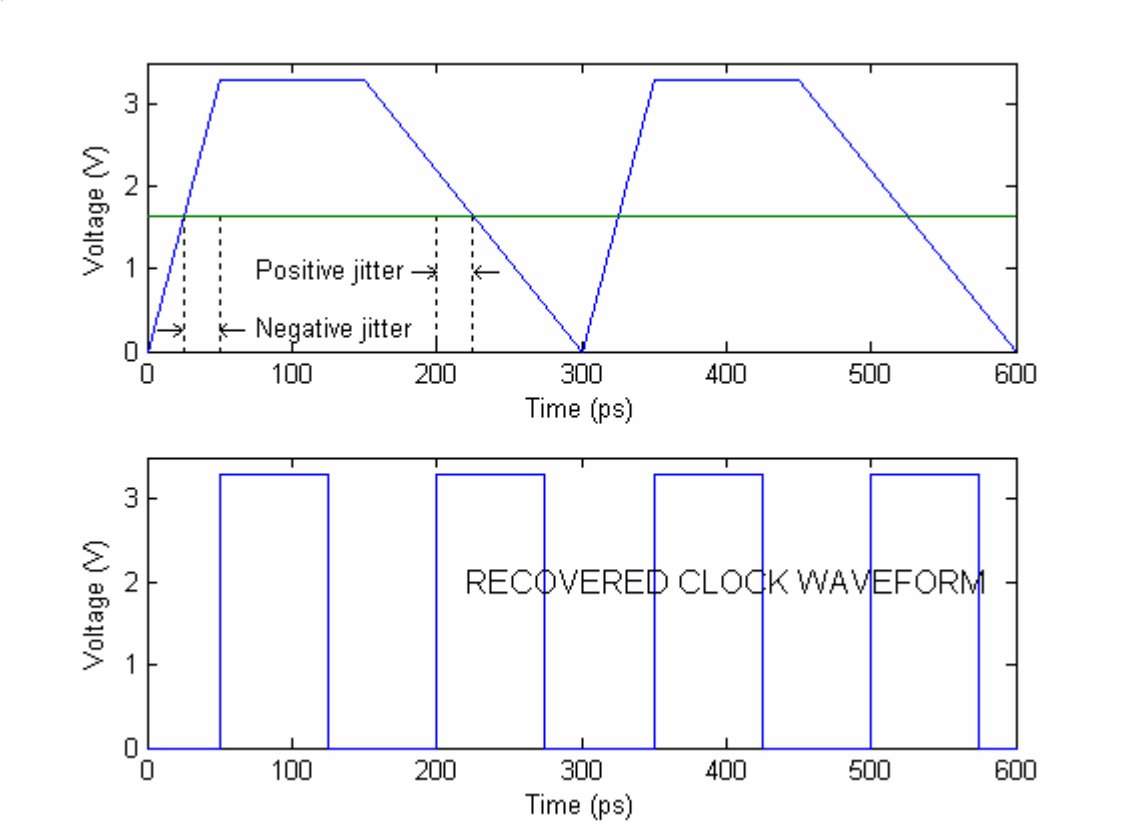


**Figure 5: DCD caused by asymmetric edge rates**

Intersymbol interference (ISI) is also called data-dependent jitter. It is caused by a data rate that is too high for the analog bandwidth of a system [9]. For alternating patterns like 1-0-1-0-1-0, this means the signal does not have enough time to fully rise or fall, which results in earlier edge crossings and negative jitter. Conversely, for repeating patterns, such as 1-1-1-0-0-0, there is more time for the waveform to reach its steady state value, which causes later edge crossings and positive jitter. Figure 6 illustrates ISI, where the signal with an alternating pattern has a lower peak value and earlier transition because it never reaches its steady state value.

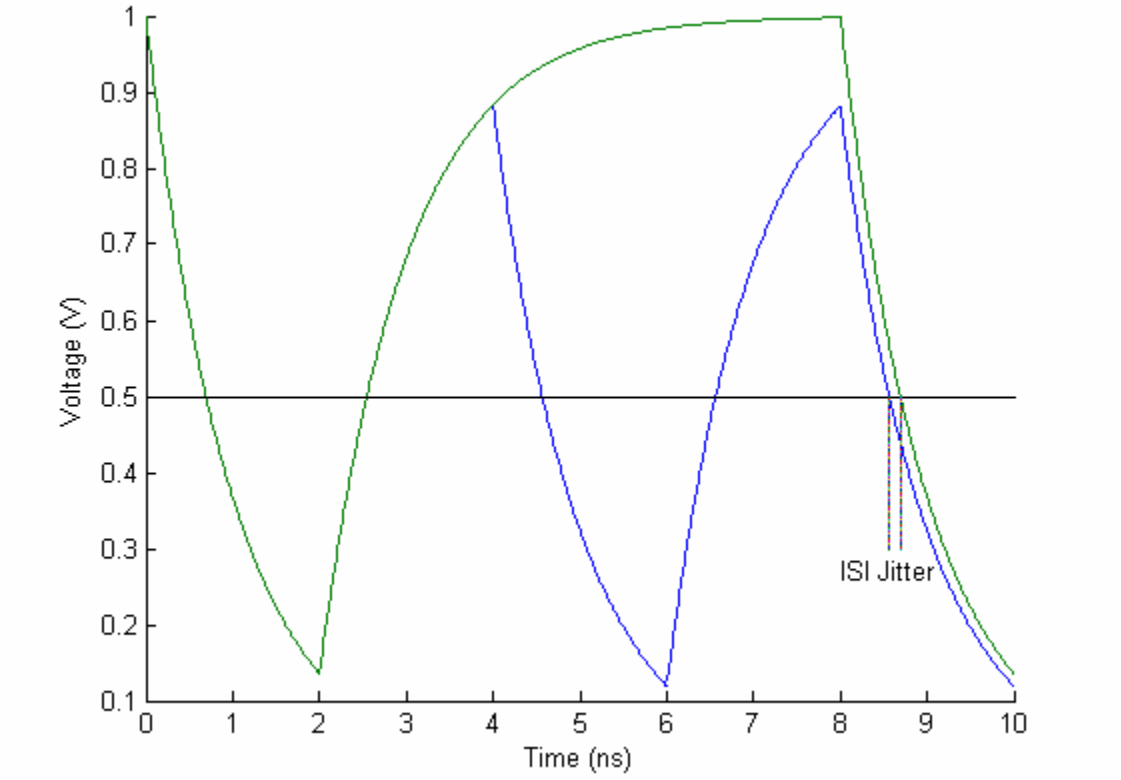


**Figure 6: Intersymbol interference**

A third type of deterministic jitter is generally caused by electromagnetic interference (EMI)[9], and is called periodic jitter (PJ) because it repeats in a cyclic fashion [11]. These cycles are based on the coupled signal's characteristics. Since any periodic waveform can be broken down into a Fourier series of individual harmonics, PJ is also known as sinusoidal jitter. A test instrument capable of performing a Fourier transform on the signal of interest is very useful for isolating this type of jitter. There are two different categories of PJ: correlated and uncorrelated [9]. Correlated jitter comes from EMI within the system, generally another signal based on the same clock. It can be tricky to isolate because its frequency spectrum characteristics may be very similar to those of the signal of interest. Uncorrelated jitter is caused by signals based on different clocks. These signals may be either internal or external to the system, but are somewhat easier to isolate because they generate frequency (spectrum) spurs apart from those caused by the signal of interest.

So, total jitter is composed of both random and deterministic components, and the three primary types of DJ are duty cycle distortion, intersymbol interference, and periodic jitter. DCD is commonly caused by an incorrect threshold level, although asymmetric edge rates can also induce it; ISI is caused by limited system bandwidth; and periodic jitter is caused by EMI. Moreover, RJ is unbounded and not correlated to the data. DJ is bounded; and, while DCD and ISI are data correlated, PJ may or may not be data correlated. These relationships are summarized in Figure 7. The next section discusses the types of jitter measurements.

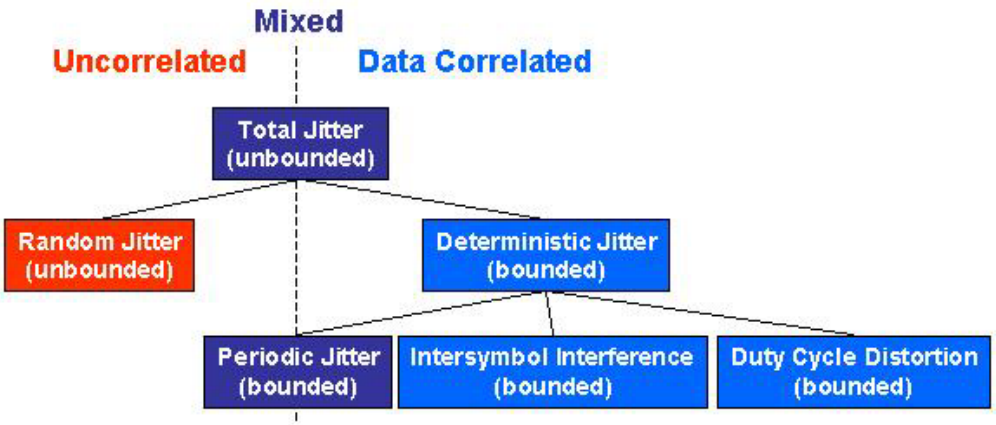


**Figure 7: Jitter decomposition chart**

# III. Jitter Measurements

Three basic jitter measurements can be performed on a single waveform: period jitter, cycle-to-cycle jitter (and a slight variant called n-cycle jitter), and time interval error (TIE) [11]. Note that there is a very subtle difference in name between two very different entities: "period" vs. "periodic" jitter. Period jitter is a *measurement*, while periodic jitter (PJ) is a type of *jitter*.

Period jitter is arguably the simplest measurement. It is computed by first measuring the period of each clock cycle in a waveform. The period jitter is the difference between the maximum and minimum periods. It can be viewed using a digital storage oscilloscope (DSO) in infinite persistence mode. The scope should be set to display a little more than one full clock period and trigger on an edge (either rising or falling). The jitter can then be seen on the edge that starts the next clock cycle [11]. Figure 8 illustrates this with a notional screenshot of a waveform triggered on the positive edge. The jitter can then be seen visually in the time distribution of the negative edge.

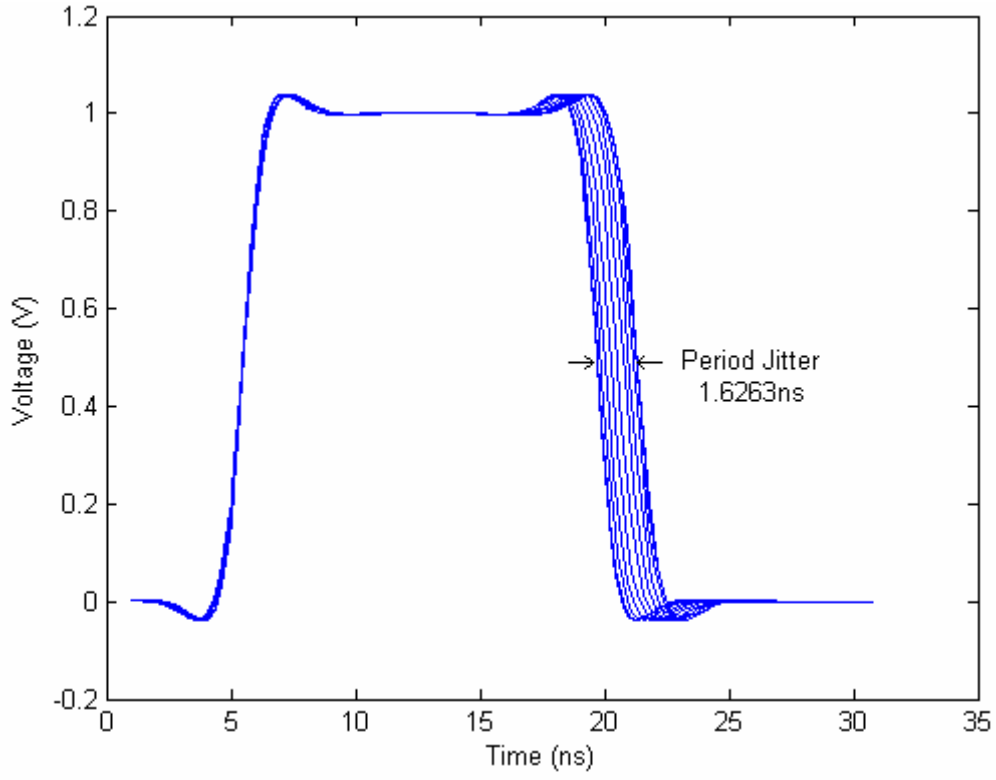


**Figure 8: Period jitter measurement**

The cycle-to-cycle jitter measurement is derived from the period jitter measurement. Cycle-to-cycle jitter is the ***difference*** in period between two ***adjacent*** clock cycles. It is useful because it reveals the short-term signal variations that a clock-recovery PLL must accommodate [11]. There is a variation of cycle-to-cycle jitter called n-cycle jitter, which measures the difference in period between ***non-adjacent*** cycles. This could be useful in a system that uses both edges of the system clock (double-data-rate, or DDR, clocking), or any other time it is important to observe timing anomalies in non-contiguous clock cycles. In the case of DDR, it might be useful to separate jitter of data clocked on the positive edge from data clocked on the negative edge (essentially 2-cycle jitter).

Time interval error (TIE) is distinctly different from period and cycle-to-cycle jitter. It is calculated by subtracting the "ideal" time of each waveform transition from the actual time of the transition (see Figure 9). Thus, the ideal transition times of the reference clock must be derived via some type of clock recovery algorithm. This can be done either with a hardware clock recovery circuit, or it can be performed by a software analysis of the captured waveform. It is worth noting that hardware clock recovery also adds jitter to the overall system, even though it is faster.

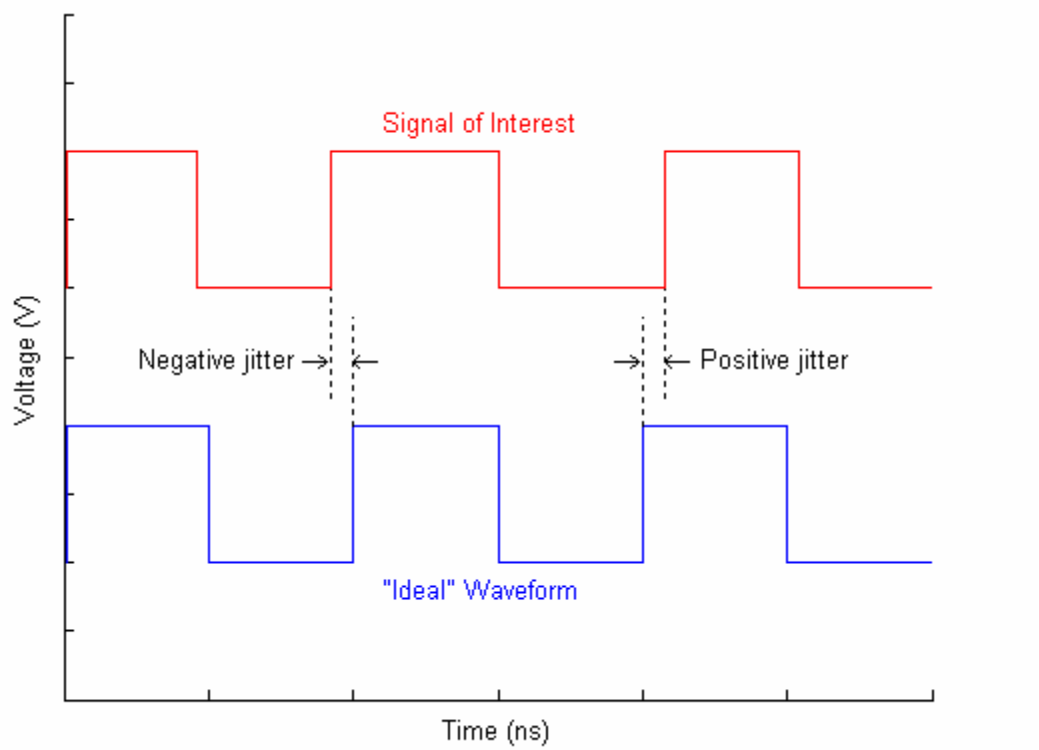


**Figure 9: Time interval error**

The period of the "ideal" reference clock is called a unit interval (UI). Although it is a much more complex measurement, a major advantage of TIE is that it reveals the cumulative effect of jitter over time. When total jitter reaches ±0.5 UI, the data valid region (also called the "eye") is closed and the system will experience bit errors [11]. If the magnitude of jitter increases relatively slowly over time, this problem may not be clear with a period jitter or cycle-to-cycle jitter measurement.

Once the nature of jitter itself and how it can be measured are understood, the next natural topic is how it can be displayed. There are several techniques, including the histogram, trend, frequency spectrum, eye diagram, and bathtub curve.

## IV. Displaying Jitter Measurements

Since jitter always has a random component, one common method of displaying it is the histogram. The horizontal axis represents time, centered about the expected transition time. The jitter is considered to be positive if the actual edge occurs after the ideal time and negative if the edge occurs before the ideal time. A truly continuous distribution across the time axis is not possible, so the values in time are assigned to "bins" in accordance with the resolution of the measuring instrument. The vertical axis represents the number of "hits," or occurrences, of an edge at that moment in time, as shown in Figure 1 through Figure 3. A measurement of jitter

over many transitions that is mapped into such a histogram forms a probability density function (PDF). If the measurement is sufficiently large, this PDF is a good indicator of the likelihood of jitter of a given magnitude. The statistical measures of mean and standard deviation are used to properly characterize it [11]. For deterministic jitter, the additional parameters of max, min, and peak-to-peak are also used.

Another method of displaying jitter measurements is called a "trend" waveform. It plots jitter magnitude on the vertical axis against "wall clock" time on the horizontal axis. Figure 10a shows the positive edges of a signal of interest, along with its ideal transitions; Figure 10b shows the associated trend display. Since the horizontal axes are the same, this display is very useful for correlating jitter to other signals [11]. This can be done by displaying the jitter trend and "other" waveform of interest together. If coupling from the other waveform is causing jitter, the trend display will often show maximums and minimums that correspond to transitions from the interfering waveform.

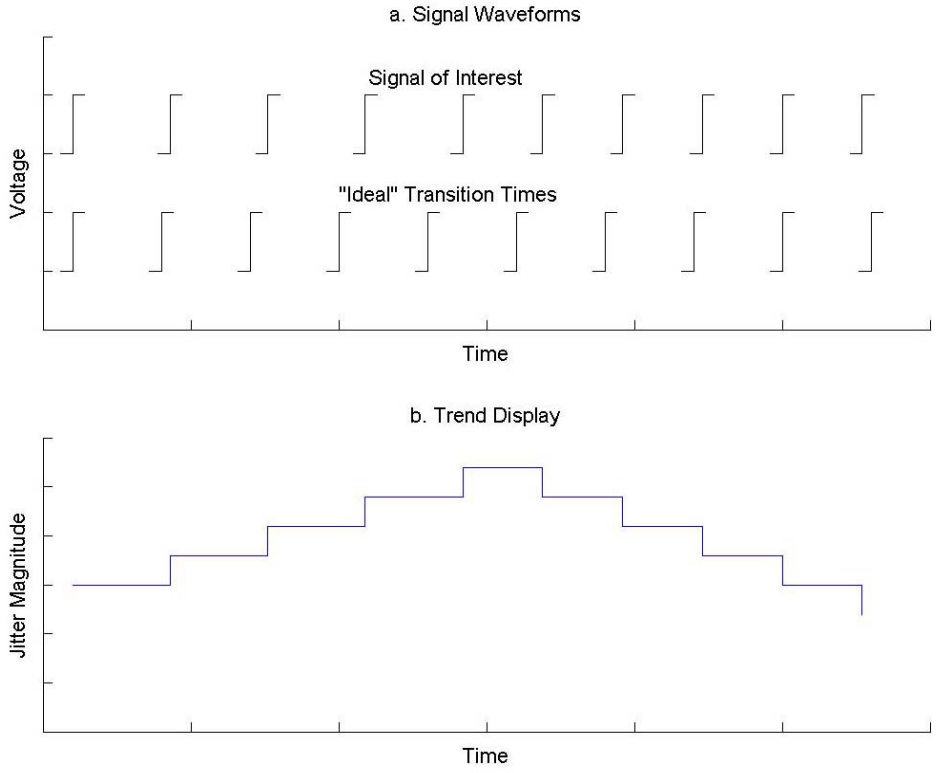


**Figure 10: Trend waveform display**

On the other hand, the trend display does a good job of revealing "trends" in the jitter (hence, its name). For instance, a common practice today is intentionally jittering a system clock to reduce its peak radio frequency (RF) energy, and thereby reduce EMI. This technique is called Spread Spectrum Clock Generation (SSCG), patented by Lexmark International [12,13]. The modulating waveform is normally a triangular wave or a close approximation thereof. Unless distorted by other sources of jitter, a trend plot will clearly reveal the modulation waveform used for SSCG.

A third technique of viewing jitter measurements is the frequency spectrum, which is a Fourier transform of the data to plot jitter magnitude on the vertical axis versus frequency on the horizontal axis. If a system is suffering EMI from an uncorrelated signal (i.e., causing uncorrelated periodic jitter), the spectrum display can be a valuable tool to help identify it [9]. (Moreover, the trend display can be used to verify it.)

A fourth measurement display is the eye diagram. It is created by overlaying many short segments of a waveform, generally just a little longer than one clock period in length, so that the ideal edge locations and voltages are aligned, as shown in Figure 11 [11]. This type of display is often generated using a real-time or sampling oscilloscope in infinite persistence mode. One advantage of the eye diagram over other types of jitter displays is that it shows time and voltage information simultaneously. The region in the middle of the eye is called the data valid window; this is where the data is stable for sampling. When a system experiences too much jitter, the data valid window shrinks to the point that setup/hold requirements are violated, causing data errors.

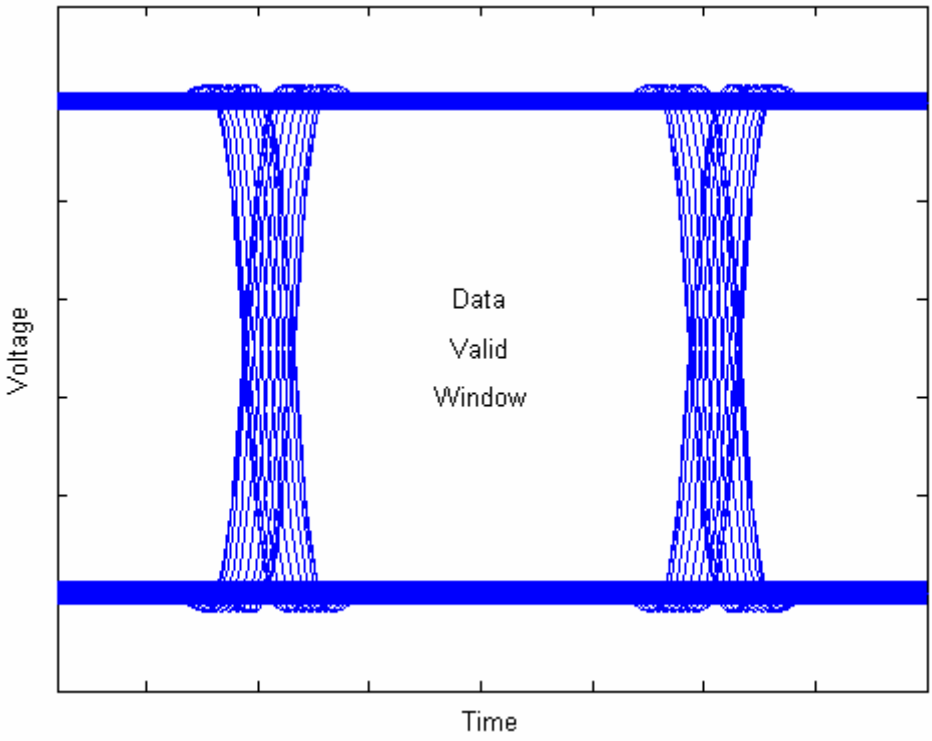


**Figure 11: Eye diagram display**

A problem with the eye diagram is that, since all jitter has an RJ component, a transition will eventually cross the data valid window within the eye. The salient question is how often that happens. If it happens once per 1000 bits, it is generally considered to be a problem. If it happens once per $10^{12}$ bits, it may be considered part of normal operation. The bit error ratio tester (BERT) can make that measurement.

Although a BERT does not measure jitter directly the way an oscilloscope or logic analyzer does, it can characterize jitter indirectly. It measures bit errors as a ratio of total bits transmitted, and produces what is known as a "bathtub" plot, as shown in Figure 12. The horizontal axis of the plot is one unit interval, and the vertical axis is the ratio of bit errors to total bits transmitted. The distance "across" the bathtub plot at a given ratio is equivalent to the width of the data valid window from the eye diagram at that data rate [11]. For example, if the bathtub plot shows a width of 0.5 UI for a bit error ratio of $10^{-5}$, then a 0.5-UI-wide data valid window on the eye diagram will (statistically) have one transition cross it out of $10^5$ transmitted bits.

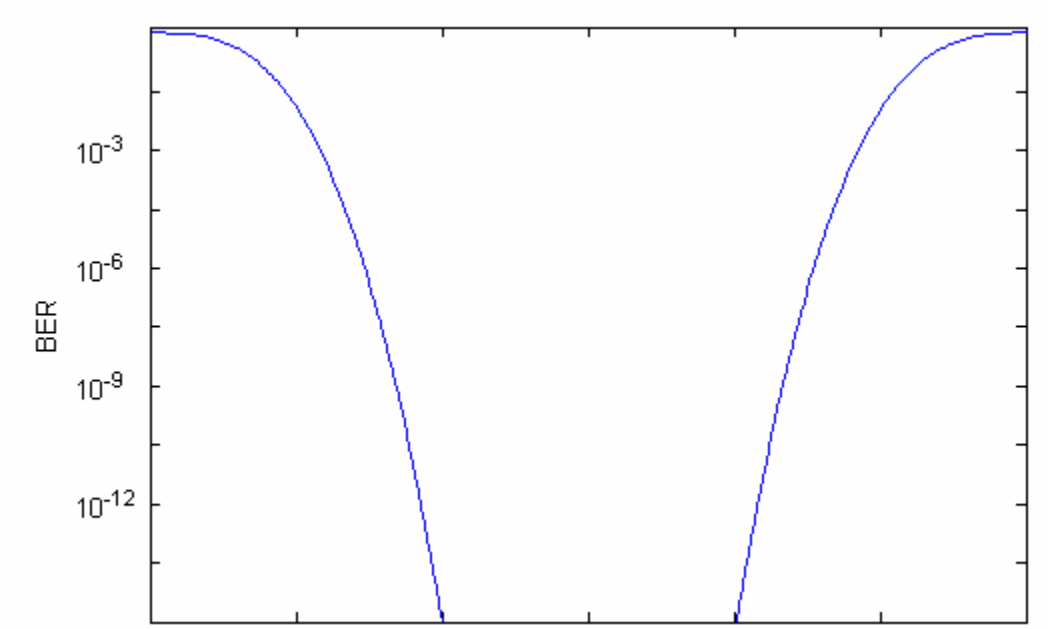


**Figure 12: Bathtub bit error ratio plot**

The bathtub plot is actually a cumulative distributive function (CDF). It comes from integrating the histograms (probability density functions) generated by measuring the jitter of the eye diagram [14]. A detailed description of the relationship between the eye diagram and bathtub plot is beyond the scope of this article, but a good description of it is given by the Wavecrest technical bulletin [15].

The next section describes some of the tools used to measure jitter.

# V. Jitter Analysis Tools

There are three basic types of measurement tools used to characterize jitter: real time, sampling, and indirect. Real time tools include standard oscilloscopes and logic analyzers. They sample each waveform at many points in order to accurately represent each captured signal. Sampling oscilloscopes typically have substantially higher bandwidth, but a much lower sampling rate, so they depend on the repetitive nature of a signal to accurately reproduce it. The BERT, as mentioned in the previous section, actually measures bit error ratio, but can use that data to derive information about jitter. Each instrument has its own advantages and disadvantages.

Perhaps one of the most common instruments used by engineers and technologists is the real time digital storage oscilloscope (DSO). Its general purpose nature and relatively low cost make it a good value for a wide variety of troubleshooting and signal characterization. Moreover, its high sampling rate normally means it is pretty fast compared to instruments that use non-real time sampling and indirect approaches. On the other hand, the DSO is also generally lower in bandwidth, and requires a specialized software package to do anything but the most basic jitter analysis.

Logic analyzers also use a real time approach to measurements. They are targeted at performing functional (logic) analysis of digital signals, tend to be more expensive, and share the real time oscilloscope's restriction of limited bandwidth. Although much less common than DSOs, logic analyzers are widely used in digital design. Moreover, with innovations of the last few years, such as Eye Finder™ and Eye Scan™ from one vendor, some logic analyzers can measure jitter quite effectively. One key advantage of the logic analyzer is that it can measure many channels simultaneously (up to several dozen, depending on the model and its configuration).

The sampling oscilloscope operates differently from a real time DSO. It essentially trades high sampling rate to get very high analog bandwidth (BW), up to dozens of GHz. A high-end sampling oscilloscope's BW is normally several times higher than the fastest DSO. Since, however, it does not sample fast enough to reconstruct a waveform from a "single shot" data capture, the sampling oscilloscope's effectiveness is largely limited to analyzing repetitive signals. It is also slower than a traditional DSO, because of lower sampling rate, and can be pretty expensive. On the other hand, for extremely fast signals, the sampling oscilloscope is one of the few tools that can do the job at all.

The principal purpose of a bit error ratio tester is different from that of an oscilloscope or logic analyzer. It compares a set of control (transmitted) data to the data received across a communications link (or bus), calculating the ratio of errors to total bits transmitted [16]. Historically, the primary graphical output of a BERT has been a bathtub plot (discussed earlier), from which jitter can be estimated. In recent years, however, innovations to the basic BERT have enabled it to do some eye characterization [16]. Although the bathtub plot is somewhat less intuitive than the graphical outputs generated by an oscilloscope or logic analyzer, the BERT has the distinct advantage of being able to perform compliance tests that other instruments simply cannot do. While oscilloscopes and logic analyzers can *estimate* bit error ratio, the BERT can *measure* it directly. Some modern communications standards specify errors on the order of one

in every $10^{12}$ bits transmitted. BERTs can prove a system's effectiveness, rather than estimate it, while also doing some jitter analysis. The downside is that it takes a long time to test terabits of data, even with a high data rate.

Yet another tool often used for jitter measurement and characterization is a time interval analyzer (TIA). TIAs measure the time difference between edges within a signal. Unlike oscilloscopes, which sample waveforms and use interpolation to estimate threshold crossing times, TIAs measure the crossing times directly. This generally means quicker test results [17]. A disadvantage of the TIA is its specialized nature; it lacks the versatility of some other test instruments.

This section and the ones before it have presented some background about the nature of jitter, how it is measured, how the measurements are displayed, and several tools that can do it. The big questions are which topics to teach in an undergraduate curriculum and when/how to teach them.

# VI. Weaving Jitter into the Curriculum

The subject of jitter analysis is a good fit for a spiral approach to education. Although in-depth jitter characterization is a complex subject, many of the basic concepts are very intuitive. Topics like the definition of jitter, why it is important, and the difference between random and deterministic jitter are easy to understand with a minimal amount of prerequisite knowledge [18, 19]. Moreover, the spiral approach to education has been used successfully for a number of years in engineering education [20, 21, 22]. In fact, the Electrical and Computer Engineering Technology department at Purdue University's College of Technology has taken this approach for several years. They use the Herrick and Jacob Series of textbooks to teach the subjects of BJTs, MOSFETs, and op amps beginning in the first semester [23, 24, 25].

In order to implement labs to support jitter education, some measurement tool must be chosen. Because of its widespread availability and familiarity, the DSO is the logical choice. Thus, this proposal is based on the assumption that DSOs are available for implementing the suggested labs. Other tools may be used, in some cases, if available.

The curriculum is divided into three phases: an introductory phase, which is qualitative in nature and focuses on conceptual understanding; a measurement and characterization phase, which is quantitative and concentrates on characterizing jitter graphically and numerically; and an analysis phase, which addresses troubleshooting to isolate different types of jitter and determine their underlying causes. These phases are intended to be split into multiple blocks of instruction taught in different semesters, although they could be combined into a single block of instruction as long as the prerequisites are covered. The following paragraphs propose topics for each of the three phases, along with the prerequisite knowledge, and laboratory suggestions to reinforce the material. The curriculum proposal is summarized in Table 1.

**Table 1: Jitter curriculum phases**

| Phase | Prerequisites | Topics | Labs |
|---|---|---|---|
| **Introduction (qualitative, year 1 or 2)** | • Real time DSO<br>• Sequential logic<br>• Rise & fall times<br>• RC circuits & exponential time constants<br>• Threshold voltage<br>• Mutual inductance & electromagnetism | • Motivation<br>• Jitter definition<br>• Jitter vs. wander<br>• RJ vs. DJ<br>• DCD/ISI/PJ definitions & causes<br>• Period jitter, cycle-to-cycle & n-cycle jitter, time interval error | • Induce DJ & observe errors<br>• Measure peak-to-peak jitter |
| **Measurement and characterization (quantitative, years 2 and/or 3)** | • Phase one topics<br>• Probability theory | • Review of jitter & measurements<br>• Displays: histogram, trend, spectrum, eye diagram<br>• Voltage noise to jitter translation<br>• Clock recovery<br>• RMS vs. peak-to-peak values<br>• Gaussian probability density function | • Measure jitter using histogram, trend, spectrum, and eye diagram displays<br>• Measure jitter induced by voltage noise<br>• Characterize jitter using peak-to-peak and RMS calculations |
| **Analysis (troubleshooting, year 3 or 4)** | • Phase one topics<br>• Phase two topics | • Review of jitter & measurements<br>• Review of displays & math<br>• Separating RJ from DJ; isolating DCD, ISI, & PJ<br>• Pseudo-random binary sequences (PRBS)<br>• 8B/10B encoding<br>• BERTs, bathtub plots, cumulative distribution functions | • Separate RJ from DJ; characterize each separately<br>• Isolate and characterize DCD, ISI, and/or PJ |

The first phase is a conceptual introduction to jitter, starting with some background information to explain why it is important, and the definitions of jitter and wander. The only prerequisite to cover these topics is an understanding of the signal transitions and timing of sequential logic in digital systems. The conceptual difference between RJ and DJ is intuitive enough that it needs no special preparation. Likewise, the jitter measurements (period jitter, cycle-to-cycle jitter, and time interval error) are intuitive and easy to explain.

On the other hand, comprehending the types of DJ and their underlying causes does require some specific preparation. To understand the causes of duty cycle distortion, one must know what a threshold voltage is, as well as the idea that signal transitions have nonzero rise and fall times. Intersymbol interference ties into both RC time constants and rise/fall times. Periodic jitter is caused by EMI, so a basic understanding of mutual inductance and electromagnetism is needed. These ideas would be reinforced with a lab that induced enough DJ into a circuit to cause errors. The students would then observe and perhaps count the errors, and use the oscilloscope in infinite persistence mode to measure the peak-to-peak jitter. Thus, the intro phase would also require experience with a DSO. These topics have been taught for the past two years, albeit without the labs, to the second-semester digital electronics class at Purdue's South Bend location [19].

Phase two would add probability theory to the prerequisites, so that the students could learn how to quantify RJ and TJ, as well as DJ. (Alternatively, the necessary probability theory could be taught as part of the EE or EET course, instead of being a separate math class.) This would include calculating RMS jitter, a discussion of the Gaussian distribution as it relates to random jitter, how to compute the amount of jitter induced by a given amount of voltage noise, and a basic clock recovery algorithm. Moreover, four of the jitter displays would be presented: the histogram, trend, frequency spectrum, and eye diagram. A lab would bolster understanding of these topics by having the students measure jitter using all four types of displays, characterize jitter with both RMS and peak-to-peak calculations, and perhaps measure the amount of jitter induced by a certain amount of voltage noise.

Depending on the program's plan of study, it may be appropriate to divide the second phase of instruction into two parts. For instance, at Purdue-South Bend the phase one material is taught during the second semester of the freshman year, but probability is not covered until the third year. Going through the entire second year with no mention of the subject of jitter would, at least to some degree, defeat the purpose of the spiral approach. Yet, second-year students are not ready for the math required to characterize RJ.

This dilemma could be handled by introducing the four displays, translation of voltage noise to jitter, and perhaps clock recovery in the second year. The displays could still be used as part of a lab, and jitter from voltage noise measured. The topics requiring probability theory would be pushed back until an appropriate time in the plan of study; possibly covered separately in the third year, or combined with the phase three subjects.

The final phase of instruction is intended for a third- or fourth-year student. It would focus on laboratory, and perhaps mathematical, techniques for separating RJ from DJ, then isolating specific types of DJ and determining the underlying causes. Additionally, the use of pseudo-random binary sequences and 8B/10B encoding would be discussed, and the BERT would be introduced. The BERT would naturally lead to a discussion of the bathtub plot (a cumulative density function) and its relationship to the eye diagram (more specifically, to its associated jitter histogram, which is a probability density function) [15]. The associated lab would consist of injecting an undisclosed (to the student) amount of jitter into a circuit, then requiring the student

to separate and characterize the various jitter components and hypothesize regarding their respective origins.

One topic remains to be addressed: assessment. Since the author and many others have seen the spiral approach work effectively with other curricula for years, there is no plan to assess the spiral approach itself. There is, however, a plan to evaluate each curriculum block at the end of the semester in which it is taught. The first of these assessments was done following the spring 2006 semester, and is being presented at the 2007 ASEE Annual Conference and Exposition [19]. It revealed a few weaknesses in the testing methodology that were corrected in the spring 2007 offering of the same course (that assessment will not be done until after this article goes online). This develop-teach-assess process will be repeated a few times, until the material is stable and its effectiveness is validated. At that time, the expectation is to incorporate assessment of the jitter curriculum into the normal course assessment. The same approach will be used for each block of lecture material and lab instruction until it all becomes a standard part of the curriculum.

# VII. Conclusion

In recent years, timing jitter has become a very significant issue in the high-speed digital electronics industry. New bus standards generally include jitter specifications that must be met for compliance. A thorough understanding of the nature of jitter, how it is measured, the different displays, and how to analyze/troubleshoot it comprise a valuable skill set for the digital systems engineer. Although timing jitter is a complex subject, many of the concepts are relatively simple, which makes it a good subject for a spiral approach, "threaded" through multiple courses in EE or EET. This article proposes a three-phase spiral approach to teaching timing jitter, beginning in the first or second year and culminating in the third or fourth year of a four-year curriculum.

Lecture materials have been developed to teach the phase one topics [18], but the labs have not yet been created. An assessment has been done of the "first trial" of the lecture material, and changes recommended [19]. Moreover, the first round of changes has been implemented. Next steps include assessing these changes, creating and implementing the phase one labs, developing phase two and three, and continuing to assess the curriculum as it evolves.

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