A 2.4 GHz High Performance CMOS Sub-Harmonic Mixer

by

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Abstract - In this paper a low power CMOS sub-harmonic mixer based on the Gilbert cell for 2.4 GHz ISM band application is presented, in which the position of the switching and transconductance stages of mixer has been exchanged. A tuning out inductor has been used between the RF and LO switching stages to improve the linearity and noise figure, and also to enhance the conversion gain of the Mixer. The utilized tuning out inductor results to higher LO voltage swing at the source terminal of RF transconductance stage transistors which provides higher conversion gain and also improves the linearity and noise performance of the mixer by tuning out the parasitic capacitances of the RF and LO stages. Simulation results performed by Advanced Design System (ADS) in TSMC 0.18 µm CMOS process at 1.8 V supply voltage show that the proposed mixer has exhibited high performance after a FOM-based comparison, without increasing the power consumption of 5 mw.

I. Introduction

In recent years, single chip low power CMOS receivers operating in the 2.4 GHz band draw great attention due to the demand of longer battery life and lower cost solutions for applications such as IEEE802.15.4, Bluetooth, and IEEE 802.11b [1]. Several receiver architectures have been presented for this target that among of them the direct-conversion receiver (DCR) is a viable candidate solution for low cost and low power single chip integration. However, DCRs have disadvantages such as local oscillator (LO) self mixing and leakage, large dc offset, and 1/f noise that can seriously degrade the performance of the receiver. To combat these problems, several techniques have been proposed such as using a frequency doubler at the output of the LO [2] and the use of a sub-harmonic mixer. In a sub-harmonic mixer, the LO frequency is internally multiplied and this mixer uses second or higher order harmonics of the LO signal for up or down conversion. Lower LO frequency significantly simplifies transceiver design, especially for blocks like frequency synthesizers, oscillators, and buffers. Hence, it

can be used to build integrated RF front-ends for high frequencies. Numerous sub-harmonic mixers were developed based on the diode nonlinearity [3, 4]. However, such mixers do not have conversion gain and require high LO power, isolator blocks, and filters making them difficult to integrate. Sub-harmonic mixers based on the modified Gilbert cell were presented in [5-8] in which an additional level of LO switching stage and quadrature LO signals rather than differential were used in order to generate the double frequency component to mix with the RF. Due to the fact that, this method needs three levels of transistors it is not suitable for low voltage applications. In [9], a BiCMOS sub-harmonic mixer was introduced in which two levels of transistors with quadrature LO signals have been used, however, the positions of the LO and RF stages have been exchanged. Therefore, it does not suffer from high supply voltage and has advantages in terms of power consumption and linearity.

For using the unlicensed 2.4 GHz ISM band, a highly linear receiver is required for immunity to the various interferer signals of different standards. The requirement of linearity performance for a mixer becomes more critical criteria in RF receivers and affects the linearity of the overall system. This requirement is approximately proportional to the dc power consumption and decreases heavily with the supply voltage. Therefore, it is a great challenge to achieve high linearity at low power and low voltage.

In this paper, a low power CMOS sub-harmonic mixer based on the Gilbert cell and by exchanging the position of switching and transconductance stages is presented with an inductor between the RF and LO switching stages to achieve higher LO voltage swing at the source terminal of RF stage transistors which provides higher conversion gain and also improves the linearity and noise performance of the mixer by tuning out the parasitic capacitances between these two stages.

II. THE PROPOSED MIXER STRUCTURE

Schematic of the proposed CMOS mixer is shown in Fig. 1. It consists of LO switching stage (M1-M4), RF transconductance stage (M5-M8), and output load stage. The LO stage is actually a frequency doubler and the currents through it are switched at twice the LO frequency. So, for using at the 2.4 GHz band, the gates of LO stage transistors are driven by 1.2 GHz quadrature signals with relative phase shifts of 0°, 90°, 180°, and 270° to effectively provide switching at twice the rate of the traditional Gilbert cell. In addition for the best noise and conversion gain performance and to make the LO stage transistors as ideal switches, these transistors are biased in the saturation region close to the triode one in order to minimize their switching time.

RF transconductance stage is in anti-parallel configuration with respect to the output or IF port while the LO switching stage is isolated from the IF port by RF differential pairs. This configuration avoids the direct coupling from the LO to RF stage, which is the origin of self-mixing, and also provides good RF-to-IF and LO-to-IF port isolation. To improve the linearity of the mixer, inductive source degeneration has been used for RF stage transistors. The degenerative inductors add very little thermal noise and have no significant cost to supply headroom. Additionally, they help in the RF port matching to standard 50 Ω

by essentially providing additional phase lag between the applied gate voltage and the device current.

The equivalent circuit for input matching of the proposed mixer with inductive degeneration is shown in Fig. 2. The input impedance can be expressed as below;

$$Z_{in} = R_g + \frac{g_m L_s}{C_{gs}} + s(L_g + L_s) + \frac{1}{sC_{gs}} \quad (1)$$

where g_m and C_{gs} are transconductance and gate-source capacitance of RF stage transistors, respectively and R_g is the parasitic resistance of inductor L_g. The input reflection coefficient (S11) is a good measure for input matching. In most practical cases, it is not necessary to have a perfect matching and S11< -10dB which corresponds to a reflection of less than 10% is usually sufficient [11].

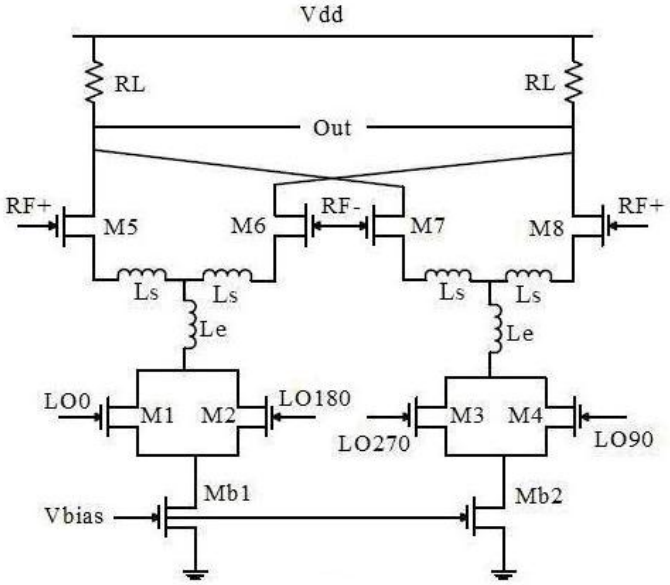

Figure 1. Schematic of the proposed mixer

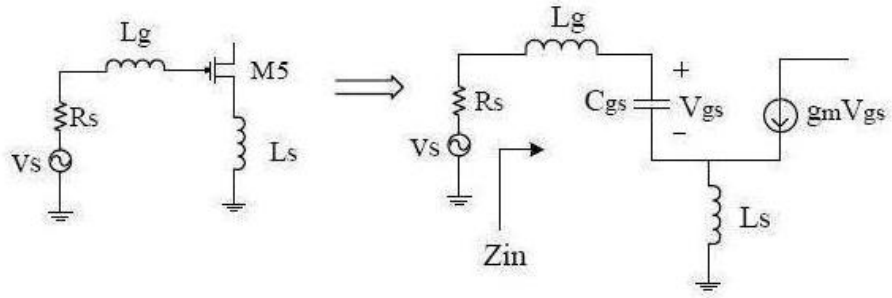

Figure 2. Equivalent circuit for input matching of the mixer

Large parasitic capacitances loading the common source of RF transconductance stage (mid-point of inductors L_s in Fig. 3) cause critical drawbacks and must be tuned out. These capacitances are nonlinear and can be charged and discharged by the offset voltage generated by mismatch and degrade the mixer linearity. In addition, they lead to reduction of the transconductance gain and cause the flicker noise such that the conversion gain and noise figure of the mixer are degraded. A simple and very effective method has been used in the proposed mixer for tuning out these capacitances by utilizing the inductor L_e between the LO switching and RF transconductance stages. The equivalent circuit which consists of parasitic capacitances $C_{p,total}$ and the tuning out inductor L_e is shown in Fig. 3. L_e in parallel with $C_{p,total}$ resonates at the desired LO frequency, which is twice the applied LO frequency, and hence the charging and discharging of the noise voltage can be suppressed leading to a significant reduction of noise figure. In addition, the tuning out inductor increases the LO voltage swing at the common source of the RF transistors, V_a, and provides higher conversion gain for the mixer at lower LO power than would be required without the enhancing inductor. The voltage at the mixing point V_a can be written as;

$$V_a = V_c + (R_e + j2\omega_{LO}L_e)i_e \tag{2}$$

where V_c is the common drain voltage of the LO transistors, L_e and R_e are the inductive value and parasitic resistance of the enhancing inductance, respectively, and i_e is the passing current through them. Since the enhancing inductor provides large impedance at the desired LO frequency, the voltage swing at V_a is larger than V_c that causes to higher conversion gain at lower LO power. Furthermore, with presence of L_e the current components at the higher order harmonics and intermodulation products are suppressed and hence the third order input intercept point (IIP3) which is a measure of linearity, is improved.

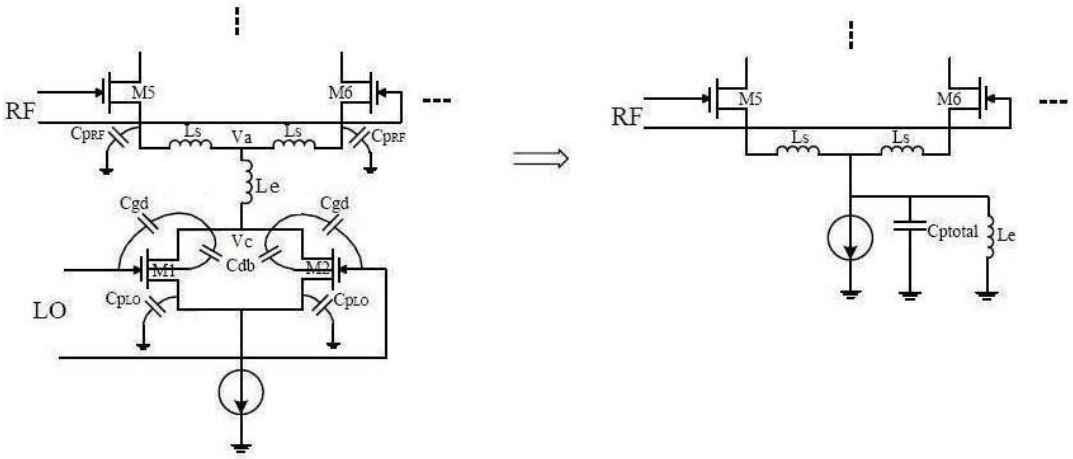

Figure 3. Parasitic capacitances of the LO stage and a method for tuning out

III. SIMULATION RESULTS

The proposed mixer is simulated by Advanced Design System (ADS) in TSMC 0.18 µm CMOS process at 1.8 V supply voltage. The RF signal at 2.41 GHz is down converted to 10 MHz through a 1.2 GHz LO signal which is doubled by the LO stage frequency doubler of the mixer. By the used input matching network in the mixer, S11 has reached to a sufficient value of -10.76 dB as shown in Fig. 4. The simulated conversion gain as a function of LO power without and with the tuning out inductor L_e is shown in Figs. 5 (a) and (b). As can be seen, by using a 4.8 nH tuning out inductor the conversion gain has been increased by 6 dB and has reached to its maximum value of 13.71 dB at lower LO power. The noise figure of the proposed mixer is 11.98 and 15.61 dB with and without L_e, respectively which indicates 3.63 dB improvement. IIP3 is set at input RF frequency of 2.4099 and 2.4101 GHz with 200 KHz separation. As shown in Fig. 6, the IIP3 of the mixer is -0.3 dBm with presence of L_e that it has been increased by 4.7 dBm in comparison with the case of without L_e.

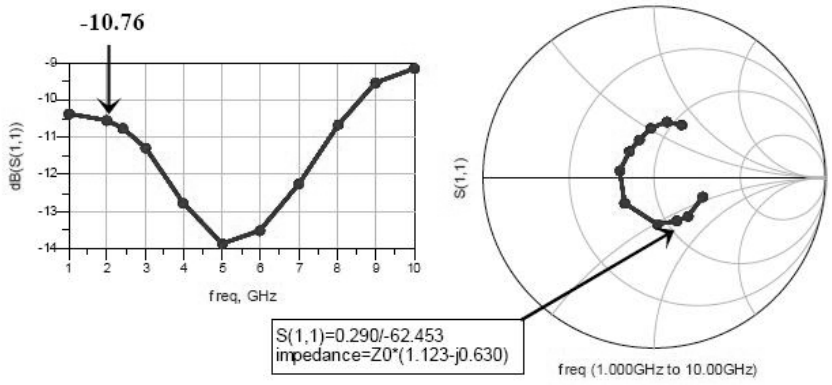

Figure 4. Simulated input matching of the proposed mixer

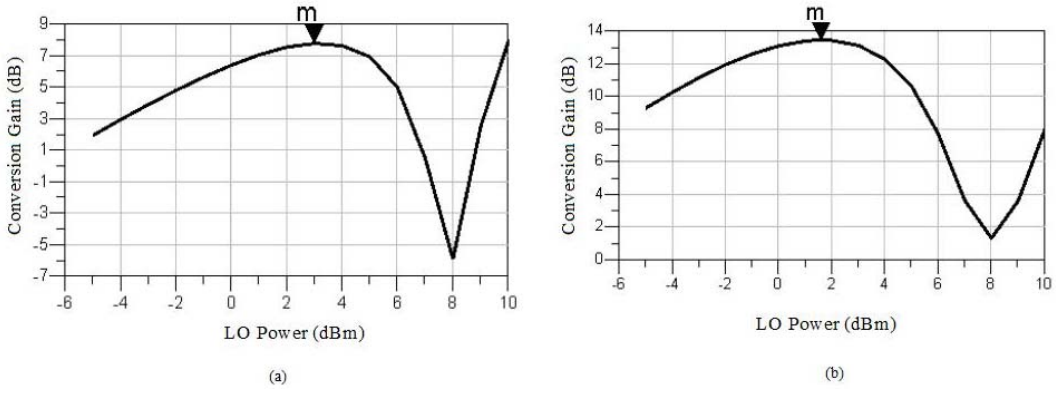

Figure 5. Simulated conversion gain versus LO power (a) without and (b) with the tuning out inductor

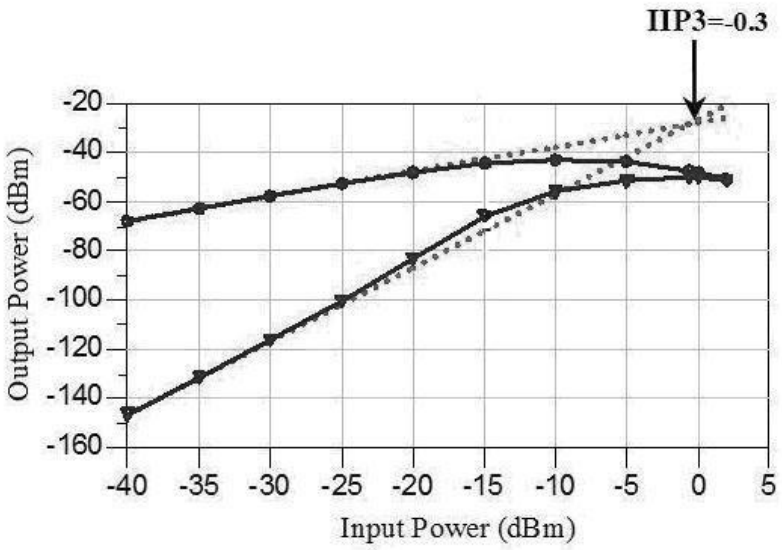

Figure 6. IIP3 of the proposed mixer

In Table I, a comparison between performance of the proposed mixer and the most recently published works is presented. A figure of merit (FOM=10log(IIP_3(mW)/P_{dc}(mW))) used in [12], is adopted here to compare the linearity of different mixers by evaluating the effect of the input third order intercept point IIP3 to the dc power dissipation. A higher FOM indicates a better linearity for mixer. By utilizing the tuning out inductor between the LO and RF stages of the proposed mixer, the linearity, conversion gain, and noise figure have been improved without increasing the power dissipation and as shown in Table I, FOM of the proposed mixer is higher than other reported mixers while its conversion gain is sufficient and consumes 5 mW power.

Table I. Performance comparison

Reference	[9]	[12]	[13]	[14]	[15]	**This work**
Technology (µm)	0.35 BiCMOS	0.18	0.18	0.18	0.18	**0.18**
Supply Voltage (V)	3	1.8	2.5	0.9	1	**1.8**
Frequency (GHz)	1.9	5.25	2.1	5.25	5.2	**2.41**
Power Dissipation (mW)	24	0.666	12.5	6.57	3.8	**5**
Conversion Gain (dB)	7.5	14.5	10.5	8.9	4.5	**13.71**
IIP3 (dBm)	-3	-17.92	-3.5	-11.66	-6	**-0.3**
Noise Figure (dB)	10	20.34	17.7	24	13	**11.98**
FOM	-16.8	-16.15	-14.47	-19.83	-11.8	**-7.29**

IV. Conclusion

In this paper, a low power CMOS sub-harmonic mixer based on the Gilbert cell for 2.4 GHz ISM band application has been presented, in which the position of the switching and transconductance stages of mixer has been exchanged. A tuning out inductor has been utilized between the RF and LO switching stages of the proposed mixer to improve the linearity and noise figure, and also to enhance the conversion gain of the Mixer that results to higher LO voltage swing at the source terminal of RF transconductance stage transistors and provides higher conversion gain and also improves the linearity and noise performance of the mixer by tuning out the parasitic capacitances of the RF and LO stages. Simulation has been done by Advanced Design System (ADS) in TSMC 0.18 µm CMOS process at 1.8 V supply voltage and has shown that the proposed mixer has exhibited high performance after a FOM-based comparison, without increasing the power consumption of 5 mw.

Acknowledgement

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Biography

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